

## Bias Resistor Transistors

PNP Silicon Surface Mount Transistors with Monolithic

Bias Resistor Network

### FEATURES

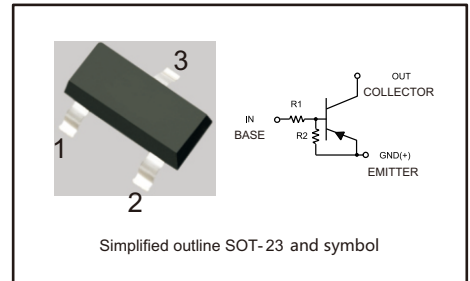
- Reduces board space
- Simplifies Circuit Design
- Reduces Board Space and Component Count

### Mechanical Data

- Case: SOT-23
- $R_1 = 1K\Omega$  (Typ),  $R_2 = 10K\Omega$  (Typ)

### PINNING

PIN	DESCRIPTION
1	BASE
2	EMITTER
3	COLLECTOR



### MAXIMUM RATINGS (Ta =25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Collector-Base Voltage	$V_{CB0}$	-50	V
Collector-Emitter Voltage	$V_{CEO}$	-50	V
Output current	$I_c$	-500	mA
Power dissipation	$P_D$	200	mW
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	625	°C/W
Junction temperature	$T_J$	150	°C
Range of storage temperature	$T_{stg}$	-55~ +150	°C

### ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted. )

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_c = -10\mu A, I_E = 0$	-50			V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_c = -1mA, I_B = 0$	-50			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	$I_E = -2mA, I_c = 0$	-5			V
Collector-Base Cut off Current	$I_{CBO}$	$V_{CB} = -50V, I_E = 0$			-100	nA
Collector-Emitter Cut off Current	$I_{CEO}$	$V_{CE} = -50V, I_B = 0$			-0.5	uA
Emitter-Base Cut off Current	$I_{EBO}$	$V_{EB} = -5V, I_c = 0$			-7.2	mA
DC Current Gain	$h_{FE}$	$V_{CE} = -5V, I_c = -50mA$	82			
Output Voltage (on)	$V_{OL}$	$V_{CE} = -5.0V, V_{BE} = -2.5V, R_L = 1.0K\Omega$			-0.2	V
Output Voltage (off)	$V_{OH}$	$V_{CE} = -5.0V, V_{BE} = -0.25V, R_L = 1.0K\Omega$	-4.9			V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_c = -50mA, I_B = -2.5mA$			-0.3	V
Input Voltage(off)	$V_{I(off)}$	$V_{CE} = -5V, I_c = -100\mu A$	-0.3			V
Input Voltage(on)	$V_{I(on)}$	$V_{CE} = -0.3V, I_c = -20mA$			-1.5	V
Input resistance	$R_1$		0.7	1.0	1.3	K $\Omega$
Input resistance	$R_2$		7.0	10.0	13.0	K $\Omega$
Resistance ratio	$R_2 / R_1$		8.0	10.0	12.0	



### Typical Performance Characteristics

Fig 1. HFE vs. IC

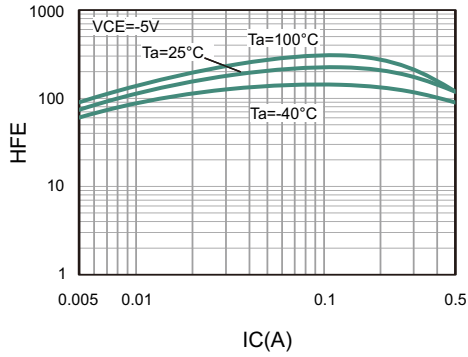


Fig 2. Vin vs. IC

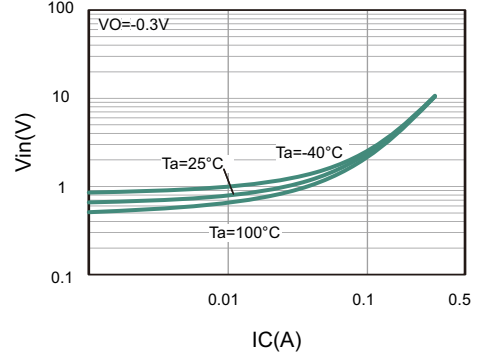


Fig 3. IC vs. Vin

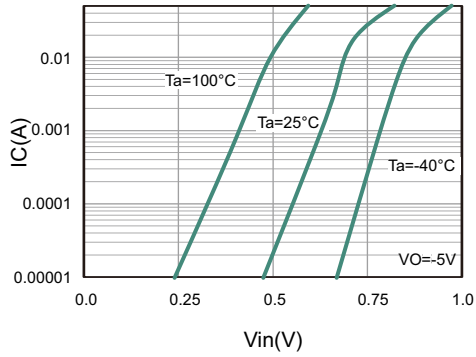
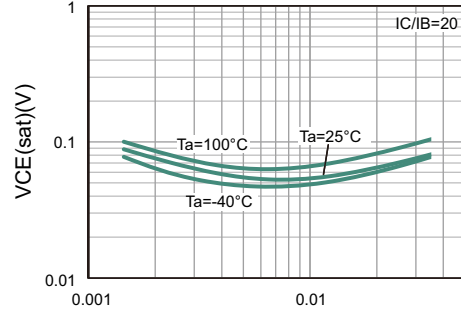
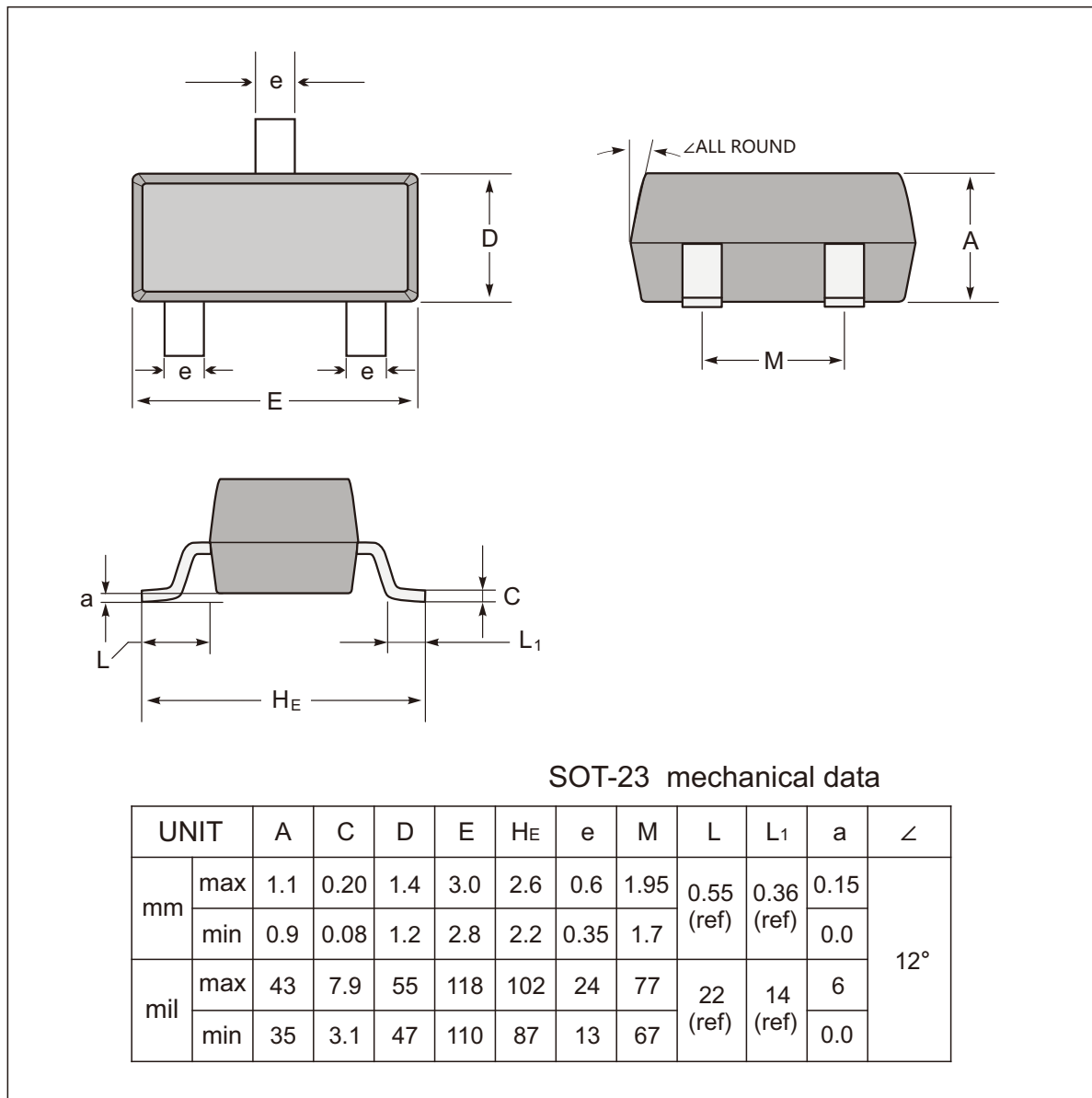


Fig 4. VCE(sat) vs. IC

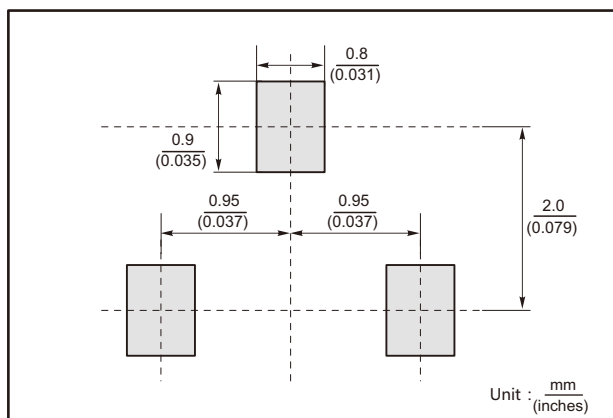




### SOT-23 Package Outline Dimensions



#### The recommended mounting pad size



#### Marking

Type number	Marking code
JDTB113ZWD	Z07



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